



# PSMN8R5-60YS

N-channel LFPAK 60 V, 8 mΩ standard level MOSFET

22 July 2015

Product data sheet

## 1. General description

Standard level N-channel MOSFET in LFPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

## 2. Features and benefits

- Advanced TrenchMOS provides low  $R_{DSon}$  and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LFPAK provides maximum power density in a Power SO8 package

## 3. Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

## 4. Quick reference data

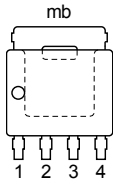
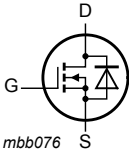
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	60	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ <a href="#">Fig. 2</a>	-	-	76	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>	-	-	106	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 100\text{ °C};$ <a href="#">Fig. 12</a>	-	-	12.8	mΩ
		$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 13</a>	-	5.6	8	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 60\text{ A}; V_{DS} = 30\text{ V};$ <a href="#">Fig. 15; Fig. 14</a>	-	7.7	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(\text{tot})}$	total gate charge	$V_{GS} = 10 \text{ V}$ ; $I_D = 60 \text{ A}$ ; $V_{DS} = 30 \text{ V}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	39	-	nC
<b>Avalanche ruggedness</b>						
$E_{DS(\text{AL})S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10 \text{ V}$ ; $T_{j(\text{init})} = 25 \text{ °C}$ ; $I_D = 76 \text{ A}$ ; $V_{\text{sup}} \leq 60 \text{ V}$ ; $R_{GS} = 50 \text{ } \Omega$ ; unclamped	-	-	97	mJ

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LPAK56; Power-SO8 (SOT669)</b></p>	 <p><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN8R5-60YS	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN8R5-60YS	8R560

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25 \text{ °C}$ ; $T_j \leq 175 \text{ °C}$	-	60	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25 \text{ °C}$ ; $T_j \leq 175 \text{ °C}$ ; $R_{GS} = 20 \text{ k}\Omega$	-	60	V

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>GS</sub>	gate-source voltage		-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>	-	106	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <a href="#">Fig. 2</a>	-	54	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	-	76	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 3</a>	-	303	A
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>slid(M)</sub>	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	76	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	303	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 76 A; V <sub>sup</sub> ≤ 60 V; R <sub>GS</sub> = 50 Ω; unclamped	-	97	mJ

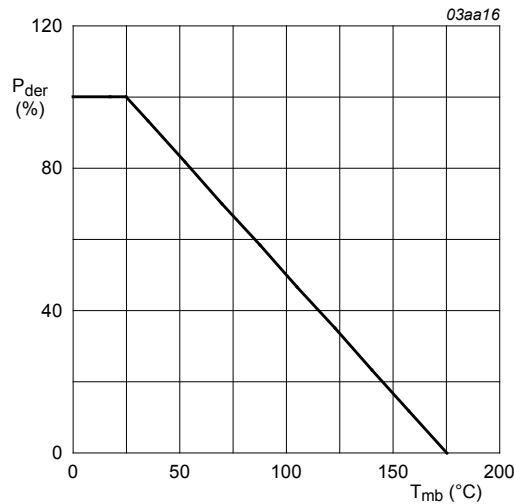


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

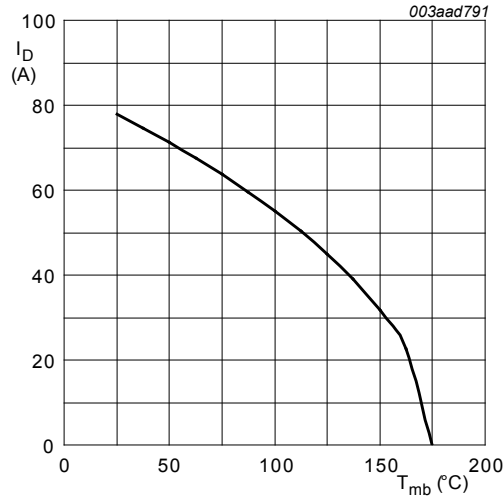


Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10 \text{ V}$$

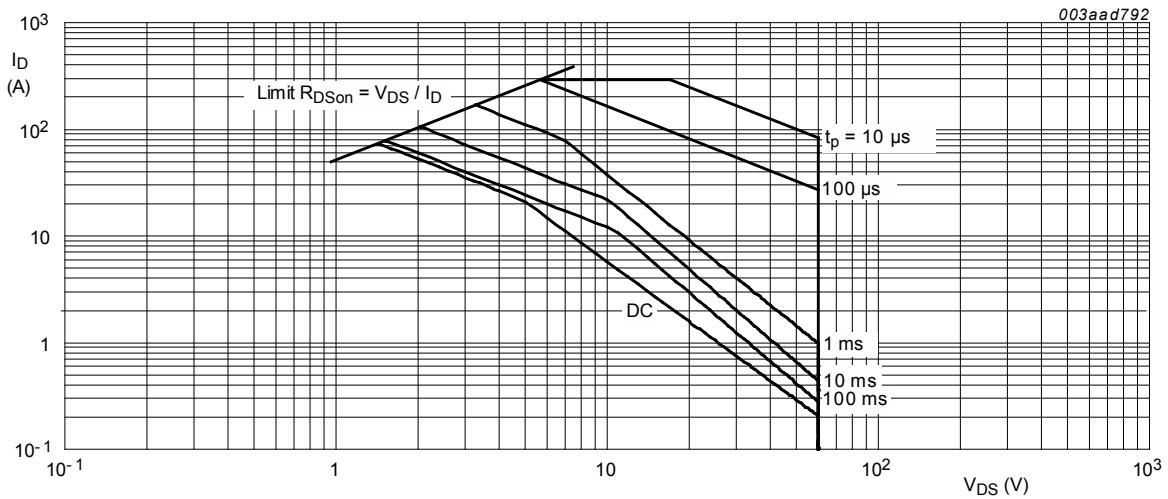


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25 \text{ }^\circ\text{C}; I_{DM} \text{ is a single pulse}$$

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.63	1.42	K/W

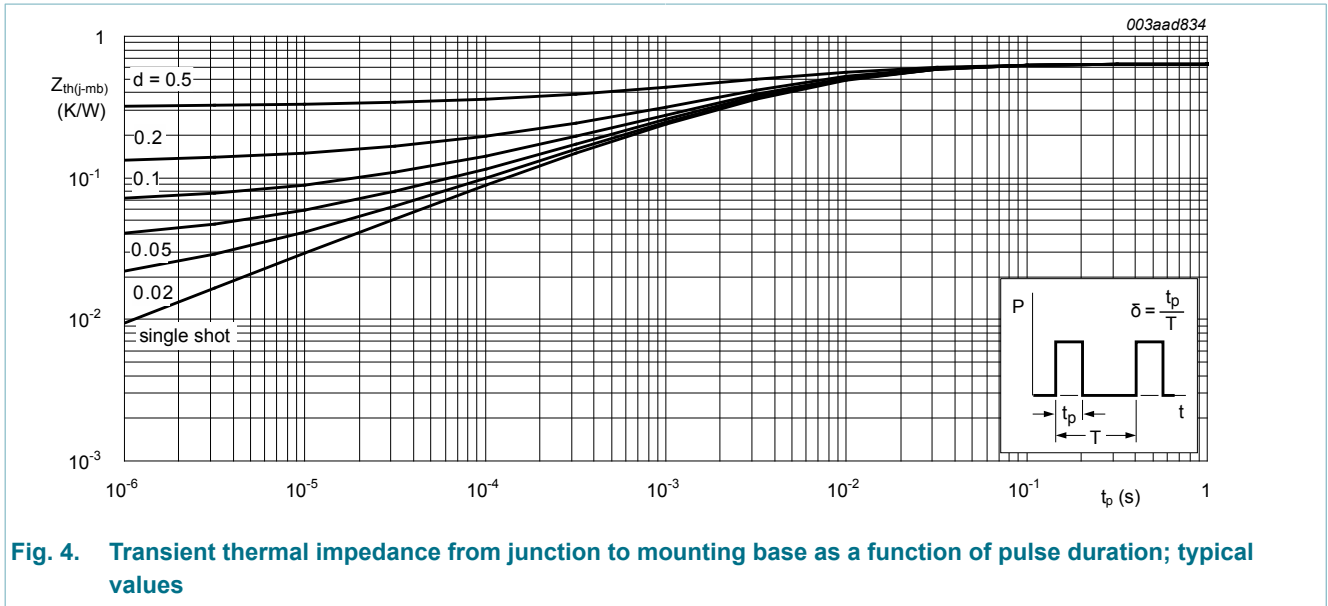


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	2	3	3.8	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; <a href="#">Fig. 11</a>	-	-	4.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 11</a>	0.95	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.03	2	$\mu A$
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	-	50	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 12</a>	-	12	18.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ }^\circ C$ ; <a href="#">Fig. 12</a>	-	-	12.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 13</a>	-	5.6	8	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	0.61	-	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 60 A; V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	39	-	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V	-	33	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 60 A; V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>	-	13.3	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge	I <sub>D</sub> = 60 A; V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 14</a>	-	7	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	6.2	-	nC
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 60 A; V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>	-	7.7	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	V <sub>DS</sub> = 30 V; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	5.2	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>	-	2370	-	pF
C <sub>oss</sub>	output capacitance		-	307	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	172	-	pF
t <sub>d(on)</sub>	turn-on delay time		V <sub>DS</sub> = 30 V; R <sub>L</sub> = 0.5 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 4.7 Ω	-	18.4	-
t <sub>r</sub>	rise time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 0.5 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 4.7 Ω	-	13.7	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	32.4	-	ns
t <sub>f</sub>	fall time		-	9.2	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 15 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 17</a>	-	0.8	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V;	-	43.3	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 30 V	-	61.4	-	nC

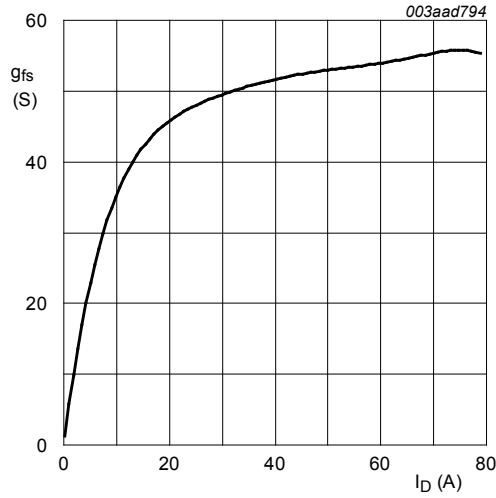


Fig. 5. Forward transconductance as a function of drain current; typical values

$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 20\text{ V}$

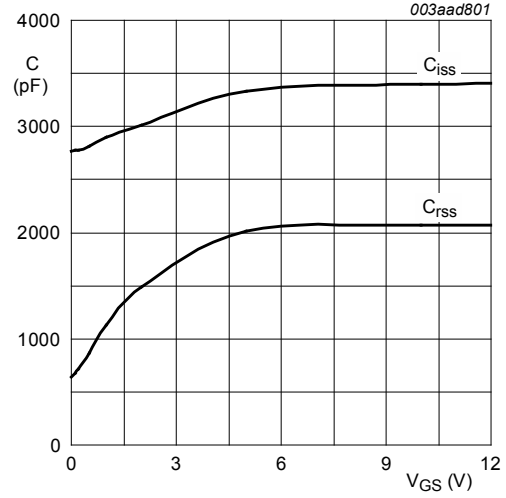


Fig. 6. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

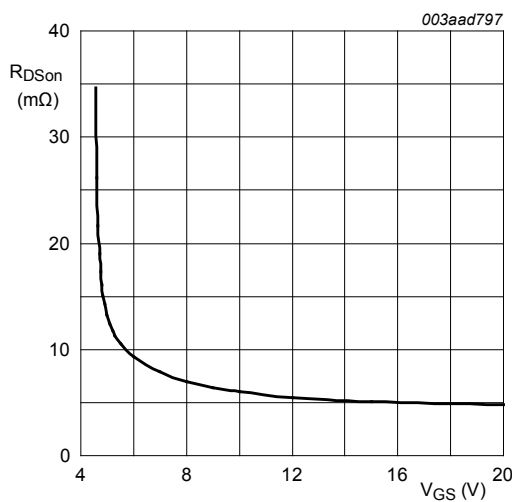


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 20\text{ A}$

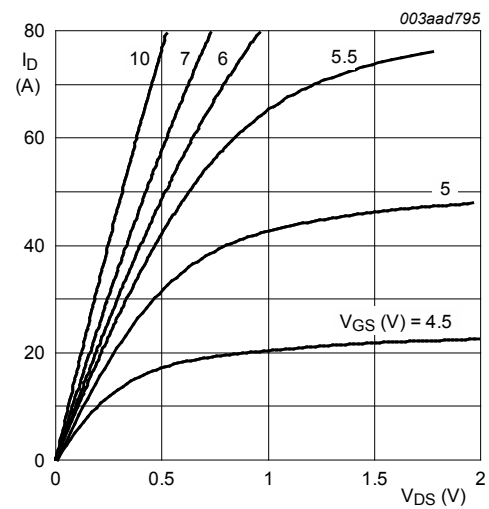
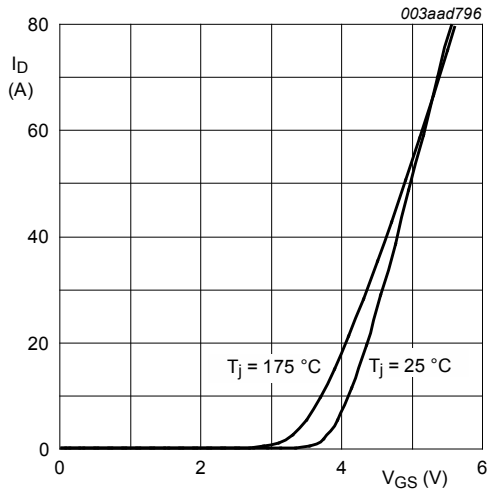


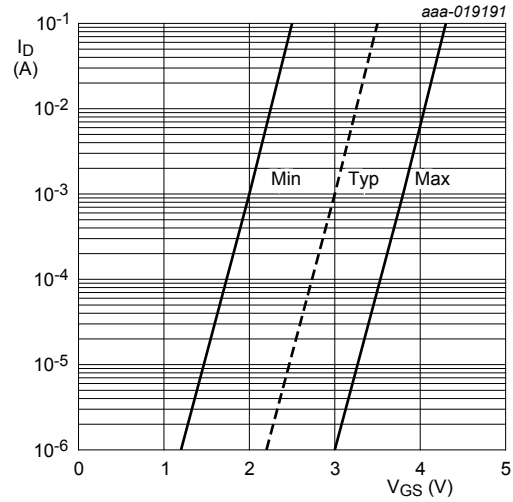
Fig. 8. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}$



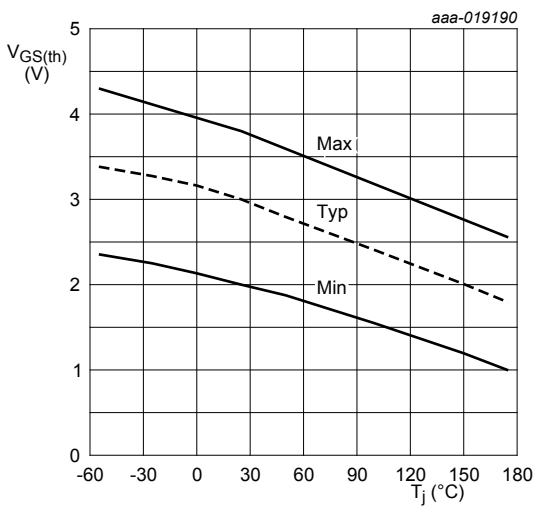
**Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values**

$$V_{DS} > I_D \times R_{DSon}$$



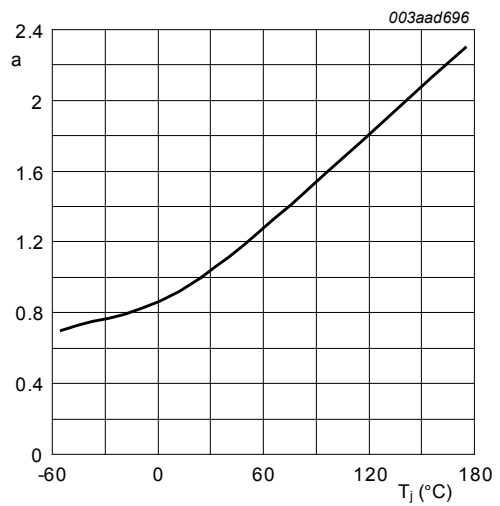
$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$

**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**



$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

**Fig. 11. Gate-source threshold voltage as a function of junction temperature**



**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature.**

$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$

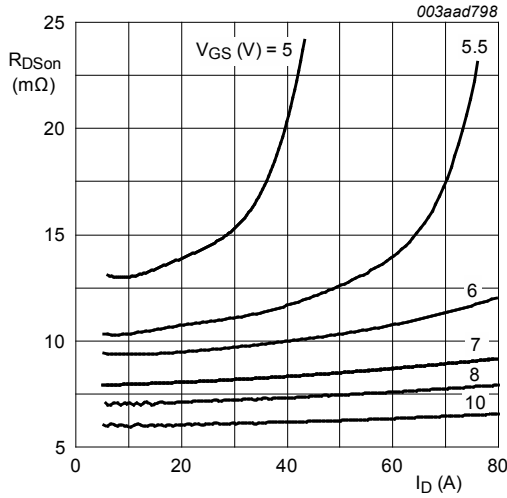


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25\text{ }^\circ\text{C}$

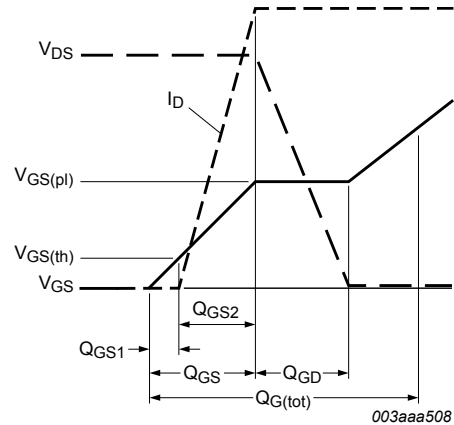


Fig. 14. Gate charge waveform definitions

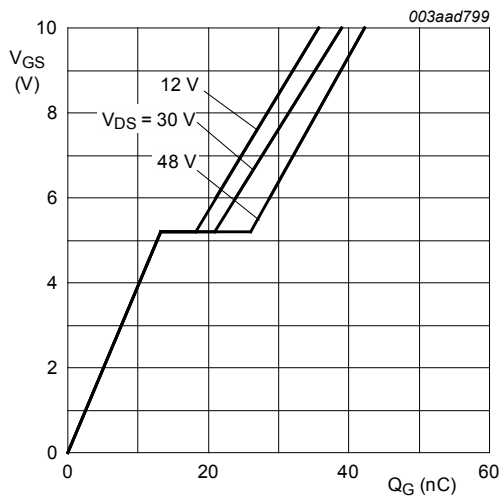


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 60\text{ A}$

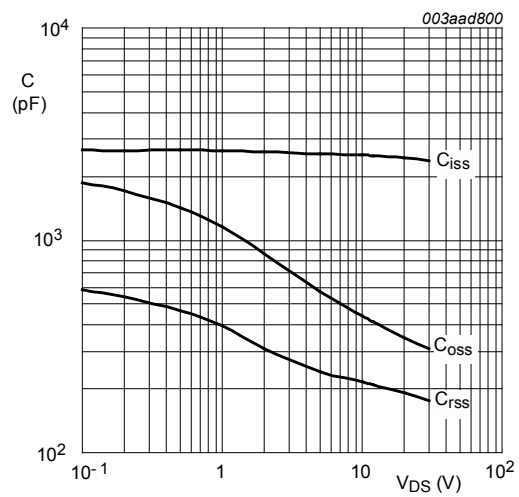


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

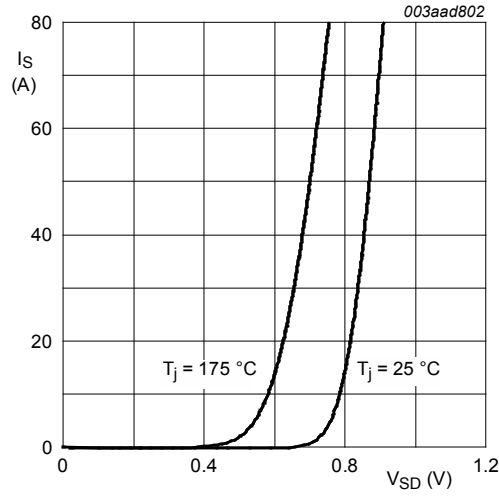
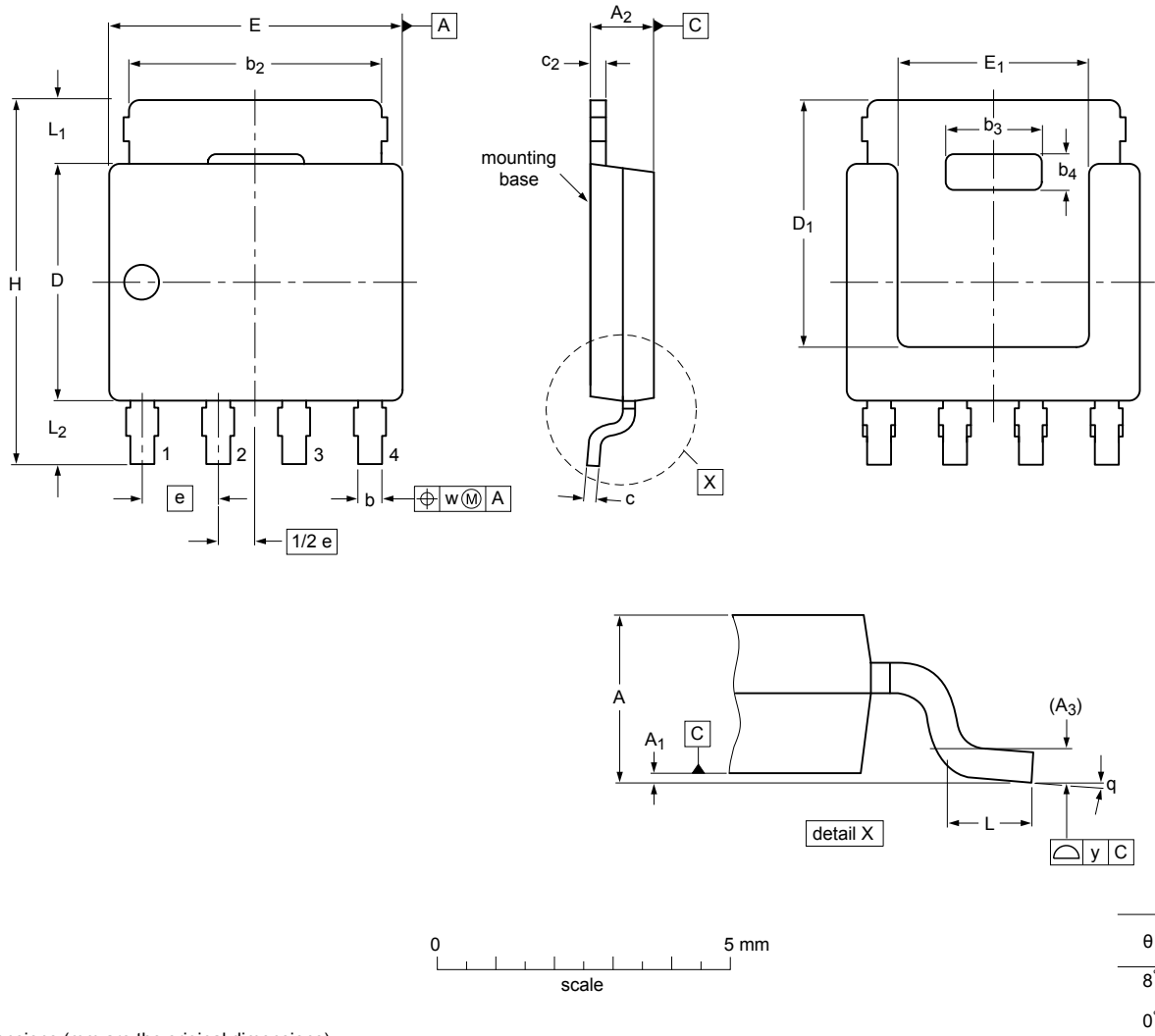


Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

### 11. Package outline

Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

Unit <sup>(1)</sup>	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3		
nom				0.25											1.27					0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				-11-03-25- 13-02-27

Fig. 18. Package outline LPAK56; Power-SO8 (SOT669)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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